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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/658,707 | 09/08/2003 | Wei-Kung Tsai | 67,200-1128 | 3171 |

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TUNG & ASSOCIATES
Suite 120
838 W. Long Lake Road
Bloomfield Hills, MI 48302

| EXAMINER | |
|---|---|
| PERKINS, PAMELA E | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2822 | |

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/658,707 | TSAI ET AL. | |
| | Examiner | Art Unit | |
| | Pamela E Perkins | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/22/04 & 6/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This office action is in response to the filing of the application papers on 8 September 2003. Claims 1-20 are pending.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 recites the limitation "the negative photoresist" in lines 9 and 13. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites the limitation "the positive photoresist" in line 10. There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Hung et al. (6,380,096).

Hung et al. disclose a method for forming a dual damascene structure semiconductor device where a via opening (104) is formed extending through at least one dielectric insulating layer (14/16/20) (col. 8, line 17 thru col. 9, line 13); blanket

depositing an anti-refelctive coating (ARC) layer (112) to include filling the via opening (104) (col. 9, lines 14-23); blanket depositing a photoresist layer (118) over and contacting the ARC layer (112) (col. 9, lines 24, 25); photolithographically patterning the photoresist layer (118) form a trench opening etching pattern (120) overlying and encompassing the via opening (104) (col. 9, lines 26-43; col. 11, lines 26-43); etching back the ARC layer (112) to form a via plug having a predetermined thickness partially filling the via opening (104), wherein the via plug is formed to fill the via opening to a level at about where a bottom portion of the trench opening (22) is formed; and etching a trench opening (22) according to the trench opening etching pattern (120) (col. 11, line 44 thru col. 12, line 16). Hung et al. further disclose carrying out a plasma ashing process to remove remaining portions of the ARC layer (112) and the photoresist layer (118) (col. 5, lines 52-65).

Hung et al. also disclose the at least one dielectric insulating layer (14/16/20) comprises a lower dielectric insulating layer (14) and an upper dielectric insulating layer (20) separated by a middle etch stop layer (16) and an uppermost dielectric layer (20) of the at least one dielectric insulating layer (14/16/20) is provided with an overlying bottom anti-reflective coating (BARC) layer (94), wherein the BARC layer (94) is etched through to expose the at least one dielectric insulating layer (14/16/20) during the step etching back and comprises at least an inorganic layer selected from the group consisting of silicon oxynitride, silicon oxycarbide, and titanium nitride (col. 8, lines 27-64). Hung et al. disclose the steps of etching back and etching a trench opening (22)

are carried out in-situ according to a plasma assisted etching process (col. 10, lines 36-58).

Although, layer 112 is described as an ARC layer, it is disclosed in the specification that layer 112 is used in a photolithographic process and therefore it is inherent that layer 112 is a photoresist layer (col. 11, lines 26-43).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al. in view of Ma et al. (6,764,810).

Hung et al. disclose the subject matter claimed above except performing at least one a photo-curing and a thermal curing process to harden the negative photoresist according to polymeric cross-linking reactions following the step blanket depositing a negative photoresist layer, wherein the cured in a nitrogen containing ambient and the at least one dielectric insulating layer comprises a low-K dielectric insulating layer selected from the group consisting of fluorine doped silicon oxide, carbon doped silicon oxide, and organo-silane glass.

Ma et al. disclose a method for forming a dual damascene structure semiconductor device where a via opening (20) is formed extending through at least

one dielectric insulating layer (12/14) (col. 4, lines 13-18); blanket depositing a first photoresist layer (22) to include filling the via opening (20) (col. 4, lines 19-37); blanket depositing a second photoresist layer (26) over the first photoresist layer (22) (col. 5, lines 1-19); photolithographically patterning the second photoresist layer (26) form a trench opening etching pattern overlying and encompassing the via opening (20) (col. 5, lines 20-45); etching back the first photoresist layer (22) to form a via plug (24) having a predetermined thickness partially filling the via opening (20), wherein the via plug (24) is formed to fill the via opening (20) to a level at about where a bottom portion of the trench opening (28) is formed; and etching a trench opening (28) according to the trench opening etching pattern (col. 5, lines 46-62). Ma et al. further disclose carrying out a plasma ashing process to remove remaining portions of the first photoresist layer (22/24) and the second photoresist layer (26) (col. 5, lines 63-67).

Ma et al. also disclose the at least one dielectric insulating layer (12/14) comprises a lower dielectric insulating layer (12) and a etch stop layer (14), wherein the at least one dielectric insulating layer (12/14) comprises a low-K dielectric insulating layer selected from the group consisting of fluorine doped silicon oxide, carbon doped silicon oxide, and organo-silane glass (col. 3, lines 29-58; col. 7, lines 11, 12); and provides an overlying bottom anti-reflective coating (BARC) layer (16) (col. 3, lines 59-67). Ma et al. disclose performing at least one a photo-curing and a thermal curing process to harden the negative photoresist according to polymeric cross-linking reactions following the step blanket depositing a negative photoresist layer, wherein the cured in a nitrogen containing ambient (col. 6, lines 34-49).

Since Hung et al. and Ma et al. are both from the same field of endeavor, a method for forming a dual damascene structure semiconductor device, the purpose disclosed by Ma et al. would have been recognized in the pertinent art of Hung et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Hung et al. by performing at least one a photo-curing and a thermal curing process to harden the negative photoresist according to polymeric cross-linking reactions following the step blanket depositing a negative photoresist layer, wherein the cured in a nitrogen containing ambient and the at least one dielectric insulating layer comprises a low-K dielectric insulating layer of carbon doped silicon oxide as taught by Ma et al. to prevent photoresist poisoning (col. 2, lines 1-39).

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nam (KR 2002-0083525/US 2004/0121578), Liu et al. (6,323,121) and Huang et al. (6,589,881) all disclose a method for forming a dual damascene structure semiconductor device where a via opening is formed extending through at least one dielectric insulating layer; blanket depositing a first photoresist layer to include filling the via opening; blanket depositing a second photoresist layer over and contacting the first photoresist layer; photolithographically patterning the second photoresist layer form a trench opening etching pattern overlying and encompassing the via opening; etching back the first photoresist layer to form a via plug having a predetermined thickness partially filling the via opening, wherein the via plug is formed

to fill the via opening to a level at about where a bottom portion of the trench opening is formed; and, etching a trench opening according to the trench opening etching pattern.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800